ABSTRACT OF THE DISCLOSURE

The present invention aims at providing efficient bus arbitration. Counters respectively provided for an encoding section and an decoding section are started when there is input of request signal from the respective encoding section and decoding section. The counter values are outputted to respective comparators that compare the counter values with predetermined values to then output the result of comparison to an arbitration controller. The arbitration controller in turn determines priority ranks for the encoding section and the decoding section based on the signals inputted from the comparators and outputs an acknowledgement signal to the module that has the highest priority. The present invention may be applied to LSI's.